IN THE CLAIMS:

Claims 1, 5, 6 and 7 have been amended herein. All of the pending claims 1 through 7 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

**Listing of Claims:**

1. (Currently amended) A method for in situ electrical testing of a flip-chip semiconductor assembly during its manufacture, the method comprising:

providing one or more integrated circuit (IC) dice, each with a surface having interconnection bumps thereon;

providing a substrate with conductive pads deposited on a surface thereof for flip-chip attachment to the interconnection bumps of the one or more IC dice;

providing a plurality of probes for contacting the substrate;

positioning the one or more IC dice on the surface of the substrate with the interconnection bumps of the one or more IC dice in conductive contact with the conductive pads of the substrate to form the flip-chip semiconductor assembly;

contacting the substrate with the plurality of probes;

while the substrate is in contact with the plurality of probes and the one or more IC dice are positioned on the surface of the substrate, and before sealing of the one or more IC dice, electrically testing the flip-chip semiconductor assembly using the plurality of probes;

repairing the flip-chip semiconductor assembly if it fails the electrical testing, ~~the repairing~~ repairing comprising at least one of:

removing and replacing at least one of the one or more IC dice of the assembly;

repairing the interconnection bumps of the at least one of the IC dice of the assembly; and

repairing at least one of the conductive pads of the substrate;

speed grading the flip-chip semiconductor assembly; and

sealing the one or more IC dice of the flip-chip semiconductor assembly.

2. (Original) The method of claim 1, wherein providing one or more IC dice comprises providing one or more IC dice selected from a group comprising Dynamic Random Access Memory (DRAM) IC dice, Static RAM (SRAM) IC dice, Synchronous DRAM (SDRAM) IC dice, microprocessor IC dice, Application-Specific IC (ASIC) dice, and Digital Signal Processor (DSP) dice.

3. (Original) The method of claim 1, wherein providing a substrate with conductive pads deposited on a surface thereof comprises providing a substrate having conductive pads comprising a material selected from a group comprising thermoplastic epoxy and quick-curable epoxy.

4. (Original) A method for electrically testing a flip-chip semiconductor assembly during its manufacture, the assembly being formed from a substrate and one or more integrated circuit (IC) dice, the method comprising:

connecting the substrate to a test apparatus at a die-attach station;

bringing the one or more IC dice into a flip-chip-type conductive contact with the substrate while it is connected to the test apparatus at the die-attach station to form the flip-chip semiconductor assembly; and

electrically testing the assembly at the die-attach station using the test apparatus.

5. (Currently amended) The method of claim 4, wherein ~~the act of~~ bringing the one or more IC dice into a flip-chip-type conductive contact with the substrate comprises pressing the one or more IC dice against a surface of the substrate so interconnection bumps on the one or more IC dice are in conductive contact with conductive pads on the surface of the substrate.

6. (Currently amended) The method of claim 4, wherein ~~the act of~~ bringing the one or more IC dice into the flip-chip-type conductive contact with the substrate comprises flip-chip-attaching the one or more IC dice to the substrate.

7. (Currently amended) The method of claim 4, wherein, ~~the~~ bringing the ~~IC die~~ one or more IC dice into a flip-chip-type conductive contact with the substrate comprises:

aligning interconnection bumps on the one or more IC dice with conductive pads on electrical pads on the substrate; and

contacting the aligned interconnection bumps on the one or more IC dice with the conductive pads on the electrical pads on the substrate to form electrical connections therebetween.